A Metric-Guided Circuit Design Methodology for Aging Guardband Compensation

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***Abstract*—This paper presents a new design methodology using gate sizing metrics for aging guardband compensation. The proposed metrics provide an efficient guardband reduction with low area overhead. Heuristics to select the best gates to be sized are proposed. The proposed design methodology has been compared against optimization using an exact method. Experimental results on ISCAS85/89 benchmark circuits show that the proposed methodology provides results close to the exact method with significant lower computational time.**

I. Introduction

Bias Temperature Instability (BTI) is a major reliability issue that increases devices threshold voltage (Vth), which in turn degrades delay. Large guardbands are usually added to the clock period to assure reliable operation. Gate sizing is an effective technique to compensate guardbands. There exist two main gate sizing approaches: *Exact Methods* [1] [2] that guarantee finding an optimal solution and *Heuristic Methods* [3] where optimal solutions are not guaranteed, but computational effort is lowered.

This paper presents a design methodology using gate sizing metrics for aging guardband compensation. The proposed metrics are used to size-up gates in the Critical Paths that impose guardbands larger than the guardband constraint (GB_C) to the clock period (Slow-CPs) to improve their aged delay, and to sized-down gates in the critical paths that have some positive slack to work properly for longer time [4] (Fast-CPs) to mitigate area overhead. The proposed methodology has been compared against optimization using an exact method. Experimental results on $ISCAS85/89$ benchmark circuits show that the proposed methodology provides results close to the exact method with significant lower computational time.

II. Proposed Gate Sizing Metrics

The following metrics are proposed to measure the benefit of sizing a gate on circuit delay and area:

$$M_{SU,i} = \frac{S^D_{Ki,AVG} \cdot |Slack^-_{i,AVG}| \cdot N_i}{\Delta A_i} \tag{1a}$$

$$M_{SD,i} = \frac{Slack^+_{i,AVG} \cdot \Delta A_i}{S^D_{Ki,AVG} \cdot N_i} \tag{1b}$$

where $M_{SU,i}$ and $M_{SD,i}$ are the metric scores for sizing-up and sizing-down the gate i, respectively. M_{SU} is evaluated on the Slow-CPs and M_{SD} is evaluated on the Fast-CPs. $S^D_{Ki,AVG}$ is the average delay sensitivity of the paths passing through the gate i to the gate size (Ki), $Slack_{i,AVG}$ is the average slack of the N_i paths passing through the gate and ΔA_i is the area cost of sizing the gate.

The benefit of taking into account each of the metrics parameters has been evaluated. Figure 1 shows the delay to area change ratio of an ad-hoc circuit obtained after sizing the gates with the highest metric score for each design action. As can be seen, as each parameter is included in the metrics, $\Delta D/\Delta A$ increases for the sizing-up design action, while it reduces for the sizing-down design action. These results show that the proposed metrics allow to select the most efficient gates for the corresponding design action.

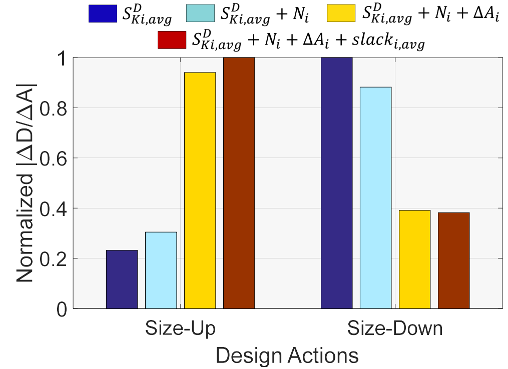

Figure 1. Metrics Validation

III. Proposed Metric-Guided Design Methodology for Aging Guardband Compensation

The proposed methodology is illustrated in Figure 2.

A. Aging-Aware Timing Analysis

The gate library is pre-characterized using polynomials. Gate delays are modeled using the following linear approximation:

$$D_{aged} = D_n + \sum_{m=1}^{M} S^D_{V_{th,m}} \cdot \Delta V_{th,m} \tag{2}$$

where D_n is the nominal gate delay, M is the number of devices in the gate, $S^D_{V_{th,m}}$ is the gate delay sensitivity to V_{th} shifts in the m_{th} device ($\Delta V_{th,m}$). ΔV_{th} of each device has been predicted using the model of [5].

Path-based aging-aware timing analysis is performed to compute the required circuit guardband (GB) to tolerate aging. If GB is larger than a maximum acceptable guardband constraint defined by the user (GB_C), a metric-guided sizing procedure is carried out.

Table I
EXPERIMENTAL RESULTS ON ISCAS BENCHMARK CIRCUITS

Circuit	CPs	CGs	50% GB Compensation				75% GB Compensation			
			Exact Method		Prop. Heuristic		Exact Method		Prop. Heuristic	
			Area (%)	CPU (*sec*)	Area (%)	CPU (*sec*)	Area (%)	CPU (*sec*)	Area (%)	CPU (*sec*)
C880	1150	102	22.06	692.61	25.21	19.65	60.61	3030.99	68.33	55.29
C1908	6770	189	17.93	6071.87	21.76	74.65	42.19	14681.3	49.84	137.41
C2670	478	104	14.29	427.41	14.38	23.68	29.71	855.55	31.80	43.75
C5315	1380	268	3.19	2625.53	3.57	48.23	6.99	5996.89	6.63	83.82
C7552	5453	854	1.27	9172.20	1.28	171.47	4.43	25981.4	4.57	326.21
S298	38	29	9.69	1.61	8.99	1.25	18.59	2.77	18.80	2.01
S838	64	48	0.82	11.25	1.16	1.36	3.99	16.73	3.66	1.98
S1423	497	179	5.24	378.59	5.19	30.59	8.66	696.18	9.43	55.05
Average			9.3	2422.6	10.2	46.4	21.9	6407.7	24.1	88.2

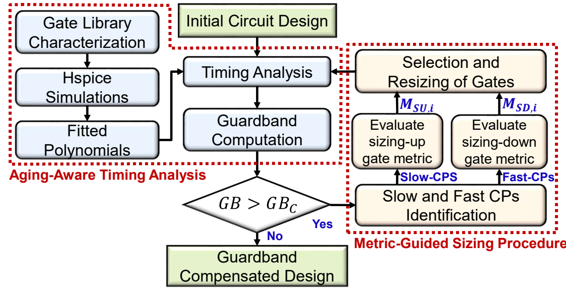

Figure 2. Proposed Methodology for Guardband Compensation using Metric-guided circuit design.

B. Metric-Guided Sizing Procedure

First, the CPs of the circuit are separated in two subsets: 1) The set of Fast-CPs requiring less guardband than GB_C for correct operation (positive slack), and 2) the set of Slow-CPs imposing larger guardbands than GB_C (negative slack). Second, the proposed metrics (Equations 1a and 1b) are evaluated for each gate. Third, based on the metrics information, the following conditions are applied to select and size gates:

Size-up condition: A gate is sized-up if it belongs to the N gates with the highest $M_{SU,i}$ score (high impact on the Slow-CPs), where N is the number of gates that can be re-sized at each iteration. The size of selected gates is increased using the following rule: $\Delta K = step \cdot M_{SU,i}$, where $step$ is a constant that defines the maximum size change.

Size-down condition: A gate is selected to be sized-down if it belongs to the N gates with the lowest $M_{SD,i}$ score (low impact on Fast-CPs). In order to limit the negative impact of sizing-down gates that also belong to the Slow-CPs, those gates with $M_{SU,i}$ higher than a constraint ($C_{M_{SU}}$) are not allowed to be sized-down. The size of selected gates is reduced using the following rule: $\Delta K = step \cdot (1 - M_{SU,i}) \cdot M_{SD,i}$.

IV. RESULTS ON ISCAS CIRCUITS

The proposed methodology for guardband compensation has been implemented in C ++ code and applied to ISCAS circuits synthesized in a Synopsys 32nm Generic Library. A lifetime constraint of 10 years has been considered.

Table I show the number of critical paths (CP) and gates (CG) for each ISCAS circuit. Different circuit sizes have been considered. Area overhead and CPU time for 50% and 75% of guardband reduction using the proposed method and an exact optimization method (penalty method) are also given. For some circuits the area overhead is high. This is because the initial designs are close to the high slope zone of the area vs delay trade-off curve. However, it can be seen that the area overhead obtained using the proposed method is very close to that obtained using the exact method. In average, 0.8% and 2.2% of extra area overhead is obtained with respect to the exact method while CPU time is improved around $52x$ and $72x$ times for a 50% and 75% of GB reduction, respectively.

V. CONCLUSION

This paper has presented a metric-guided design methodology for aging guardband compensation. Gate metrics have been proposed and validated by showing that selected gates efficiently reduce guardband with low area overhead. The metrics information is used to select both gates to be sized-up to reduce guardband and gates to be sized-down to mitigate area overhead. The proposed methodology has been compared against an exact optimization method and it has been shown that close to optimum results are obtained with significant lower computational time.

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