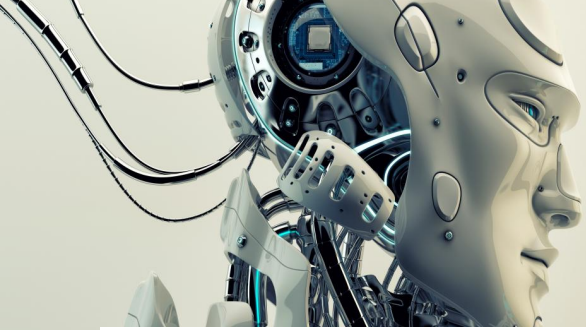

# Verification of Digital Systems

## Labs' Manual

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# Introduction

## Connecting to Lab Computers

# Contacts

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Materials: http://ati.ttu.ee/~rpi/IAF0620/PSL/

## Introduction

# Connecting to Lab Computers

- Using Linux
- Using Windows
- Using Mac OS X

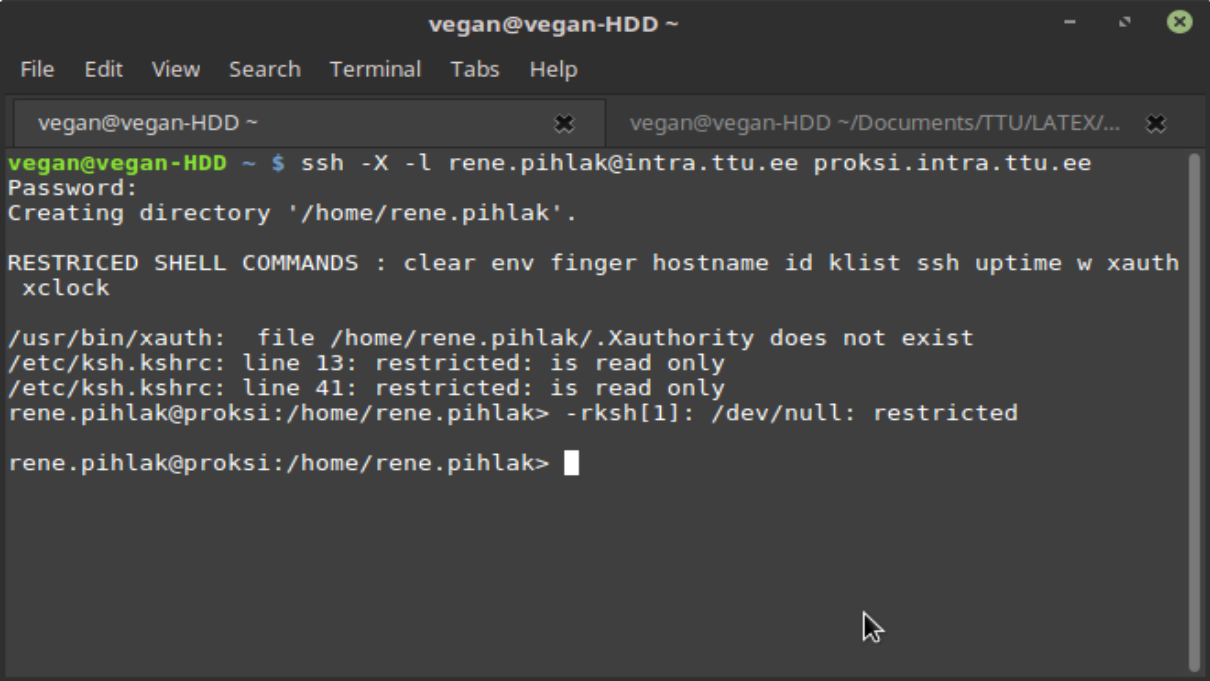
# Using Linux to Proxy Server

Connecting to lab computers requires connecting first to our proxy server. This can be done using command line by entering the following command:

```
ssh -X -l Heli.Kopter@intra.ttu.ee proksi.intra.ttu.ee
```

where

- `ssh` – secure shell,
- `-l` – lowercase 'L',
- `-X` – parameter requesting X forwarding (important!!)
- `Heli.Kopter` – your UNI-ID as login name.

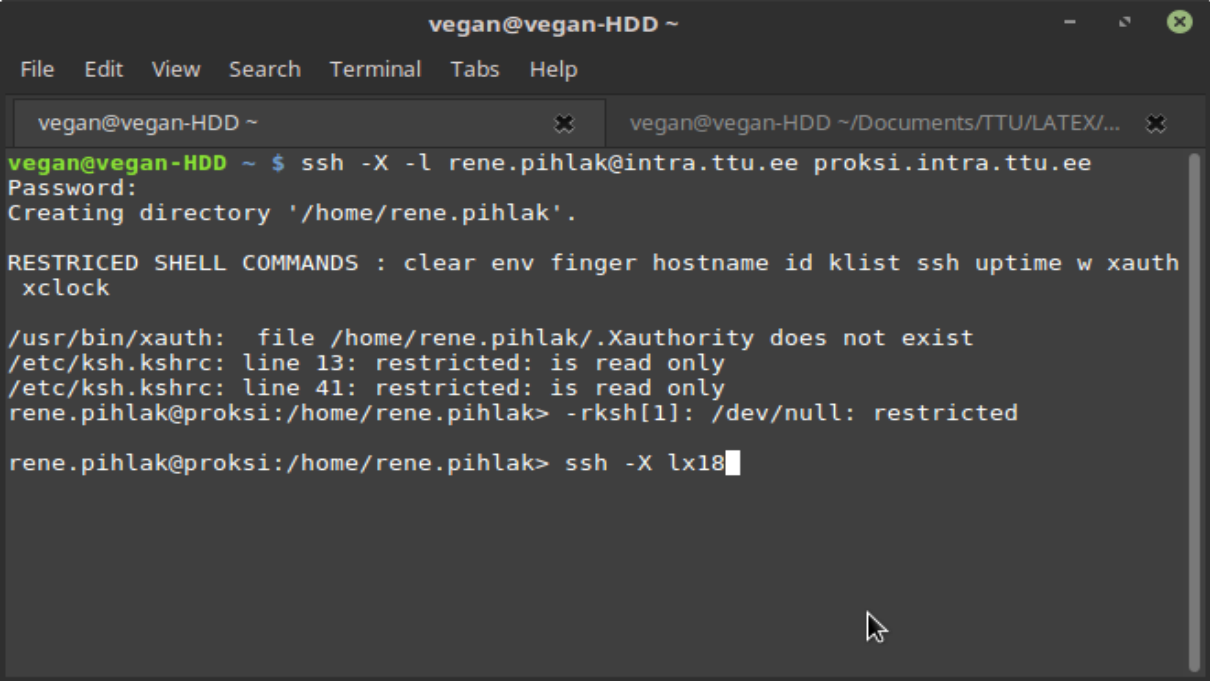

vegan@vegan-HDD ~
File Edit View Search Terminal Tabs Help
vegan@vegan-HDD ~
vegan@vegan-HDD ~/Documents/TTU/LATEX/...
vegan@vegan-HDD ~ $ ssh -X -l rene.pihlak@intra.ttu.ee proksi.intra.ttu.ee
Password:
Creating directory '/home/rene.pihlak'.
RESTRICED SHELL COMMANDS : clear env finger hostname id klist ssh uptime w xauth
xclock
/usr/bin/xauth: file /home/rene.pihlak/.Xauthority does not exist
/etc/ksh.kshrc: line 13: restricted: is read only
/etc/ksh.kshrc: line 41: restricted: is read only
rene.pihlak@proksi:/home/rene.pihlak> -rksh[1]: /dev/null: restricted
rene.pihlak@proksi:/home/rene.pihlak>

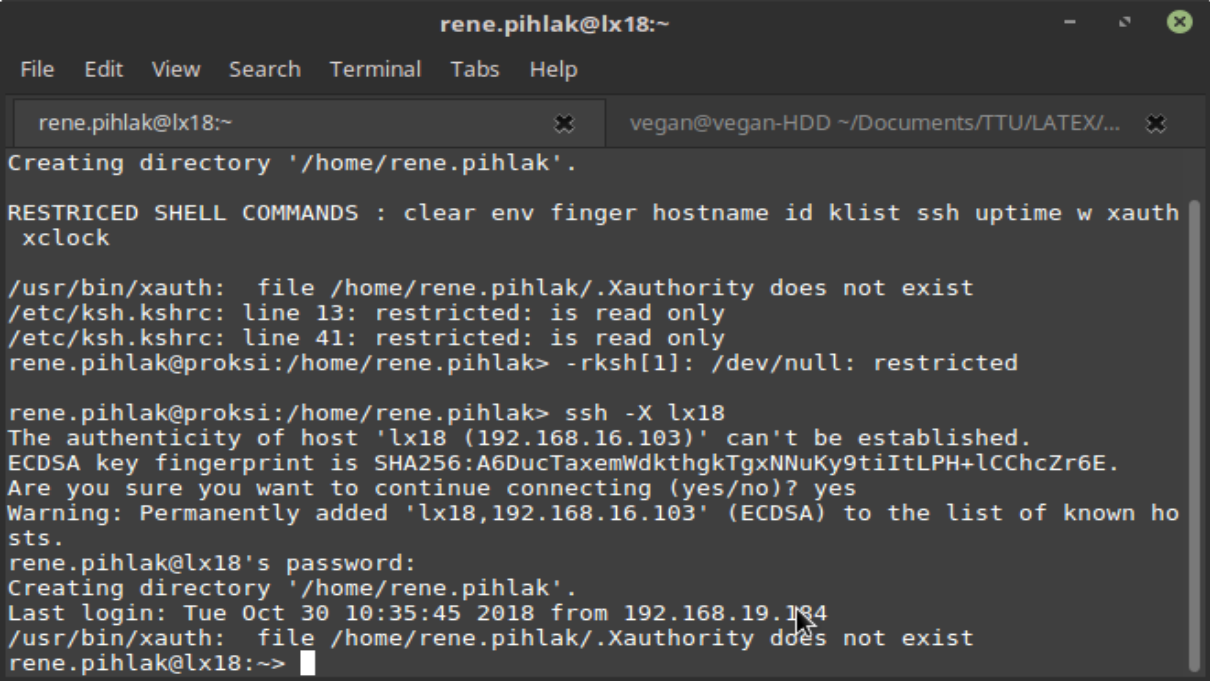
# Connect to Lab Computer

Follow the instructions (i.e. enter your password, etc).
After you have logged in to the proxy server, connect to a specific lab computer to run your programs. In order to connect to a lab computer use the following command:

```
ssh -X lx9
```

where
- `ssh` – name of the command,
- `-X` – parameter requestion X forwarding (important!!), and
- `lx9` – the ID of computer.


vegan@vegan-HDD ~
File Edit View Search Terminal Tabs Help
vegan@vegan-HDD ~
vegan@vegan-HDD ~/Documents/TTU/LATEX/...
vegan@vegan-HDD ~ $ ssh -X -l rene.pihlak@intra.ttu.ee proksi.intra.ttu.ee
Password:
Creating directory '/home/rene.pihlak'.
RESTRICED SHELL COMMANDS : clear env finger hostname id klist ssh uptime w xauth
xclock
/usr/bin/xauth: file /home/rene.pihlak/.Xauthority does not exist
/etc/ksh.kshrc: line 13: restricted: is read only
/etc/ksh.kshrc: line 41: restricted: is read only
rene.pihlak@proksi:/home/rene.pihlak> -rksh[1]: /dev/null: restricted
rene.pihlak@proksi:/home/rene.pihlak> ssh -X lx18


rene.pihlak@lx18:~
File Edit View Search Terminal Tabs Help
rene.pihlak@lx18:~
vegan@vegan-HDD ~/Documents/TTU/LATEX/...
Creating directory '/home/rene.pihlak'.
RESTRICED SHELL COMMANDS : clear env finger hostname id klist ssh uptime w xauth xclock
/usr/bin/xauth: file /home/rene.pihlak/.Xauthority does not exist
/etc/ksh.kshrc: line 13: restricted: is read only
/etc/ksh.kshrc: line 41: restricted: is read only
rene.pihlak@proksi:/home/rene.pihlak> -rksh[1]: /dev/null: restricted
rene.pihlak@proksi:/home/rene.pihlak> ssh -X lx18
The authenticity of host 'lx18 (192.168.16.103)' can't be established.
ECDSA key fingerprint is SHA256:A6DucTaxemWdkthgkTgxNNuKy9tiItLPH+lCChcZr6E.
Are you sure you want to continue connecting (yes/no)? yes
Warning: Permanently added 'lx18,192.168.16.103' (ECDSA) to the list of known hosts.
rene.pihlak@lx18's password:
Creating directory '/home/rene.pihlak'.
Last login: Tue Oct 30 10:35:45 2018 from 192.168.19.184
/usr/bin/xauth: file /home/rene.pihlak/.Xauthority does not exist
rene.pihlak@lx18:~>

# Check Status Before Connecting

Before connecting to a lab computer, please check if the computer is available (i.e. that it is running Linux) and what is the current load of the computer. You can get information about the current status of lab computers by visiting the following web page:

https://ati.ttu.ee/klassi-staatus/

This web page also provides the names/IDs of the computers.
Once you have successful logged in to a lab computer you can set up the Linux system to start using Questa Sim.

# Using Windows

If you are using Windows operating system, there are several ways to connect to the lab computers. Make sure you also read the instructions for Linux. One way to connect to the proxy server (and lab computers) can be done using program called `putty`:

http://mini.li.ttu.ee/~priit/IAY0340.2013/ssh_setup/putty_guide.html
Notice that in order to be able to see GUI applications, you might have to installe additional software such as `Cygwin` or `Xming`. Therefore the preferred and recommended way to connect is by using Linux.

# Using Mac OS X

This guide is not tested on latest Mac OS X. If the necessary X11 libraries are installed, then connecting should be identical to Linux.

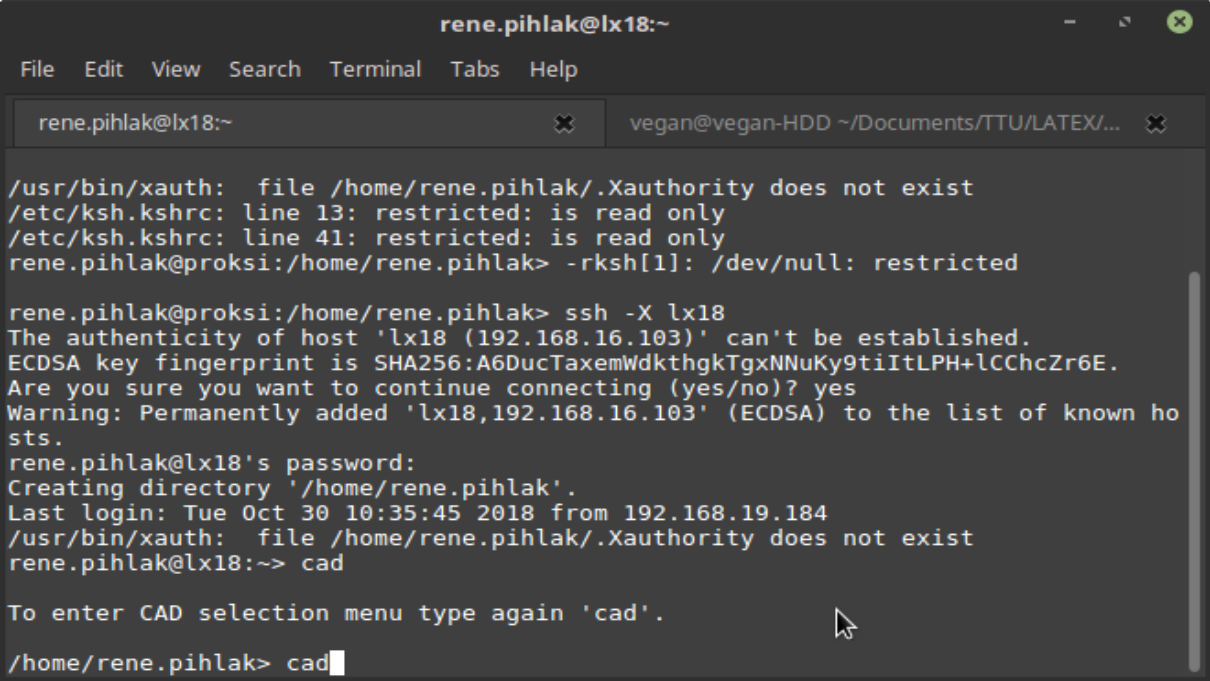
# Setting Up Linux Environment

## Setting up a project in Questa Sim

# Setting Up Lab Computer

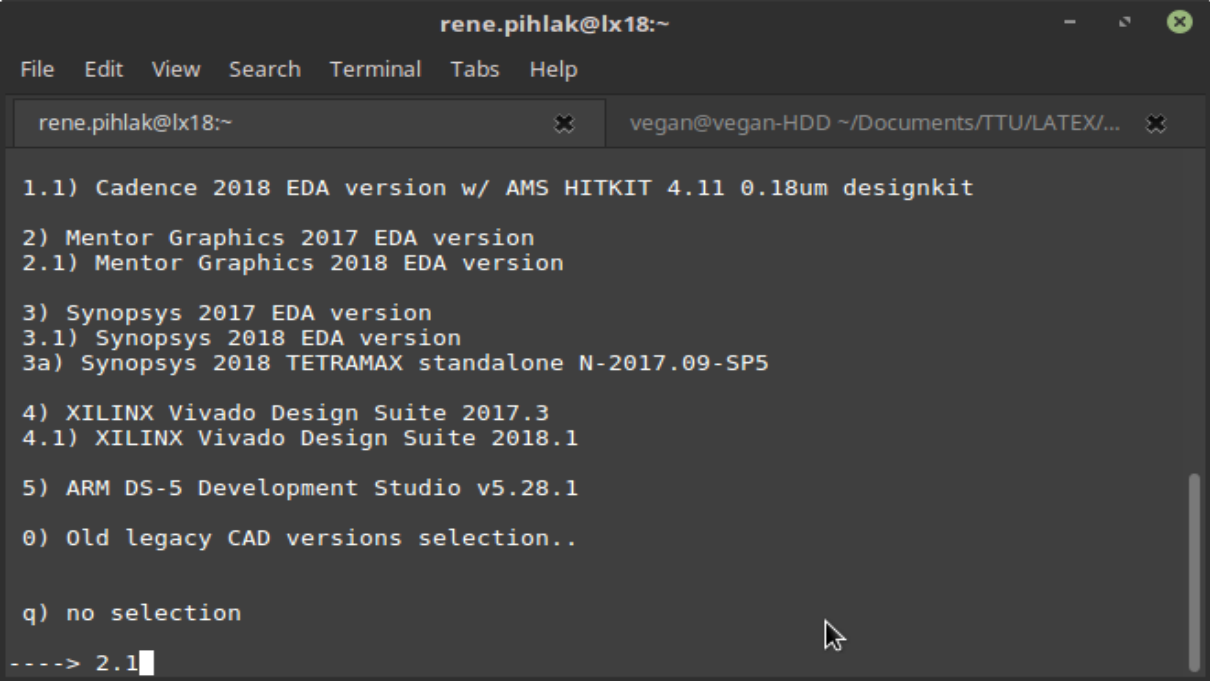
Before launching Questa Sim, the Linux environment has to be configured. This step is necessary both when using lab computers at school and when connecting to the lab computers remotely. The following example shows how to configure the system when using lab computers remotely.
After logging in to the lab computer running Linux operating system, run the following command(s) in the command line:

```
cad
cad
```


rene.pihlak@lx18:~
File Edit View Search Terminal Tabs Help
rene.pihlak@lx18:~
vegan@vegan-HDD ~/Documents/TTU/LATEX/...
/usr/bin/xauth: file /home/rene.pihlak/.Xauthority does not exist
/etc/ksh.kshrc: line 13: restricted: is read only
/etc/ksh.kshrc: line 41: restricted: is read only
rene.pihlak@proksi:/home/rene.pihlak> -rksh[1]: /dev/null: restricted
rene.pihlak@proksi:/home/rene.pihlak> ssh -X lx18
The authenticity of host 'lx18 (192.168.16.103)' can't be established.
ECDSA key fingerprint is SHA256:A6DucTaxemWdkthgkTgxNNuKy9tiItLPH+lCChcZr6E.
Are you sure you want to continue connecting (yes/no)? yes
Warning: Permanently added 'lx18,192.168.16.103' (ECDSA) to the list of known ho
sts.
rene.pihlak@lx18's password:
Creating directory '/home/rene.pihlak'.
Last login: Tue Oct 30 10:35:45 2018 from 192.168.19.184
/usr/bin/xauth: file /home/rene.pihlak/.Xauthority does not exist
rene.pihlak@lx18:~> cad
To enter CAD selection menu type again 'cad'.
/home/rene.pihlak> cad

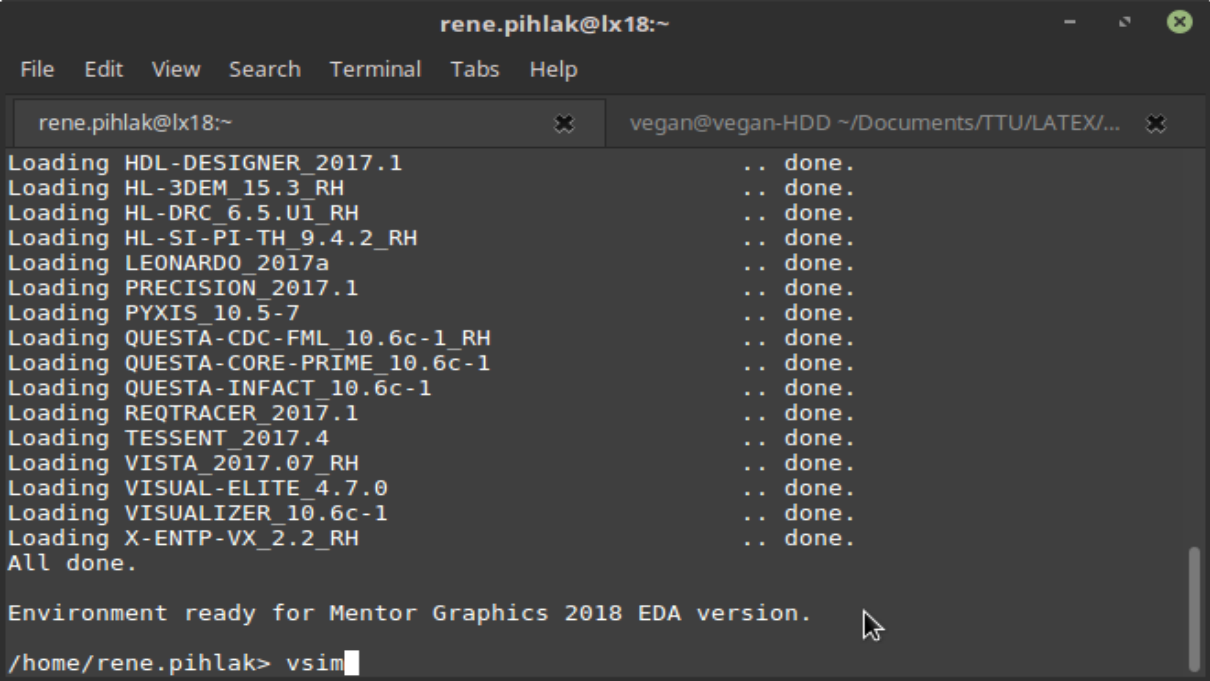
# Setting Up Lab Computer

Once the menu appears, type '2.1' to select Mentor Graphics 2018 and press ENTER.


rene.pihlak@lx18:~
File Edit View Search Terminal Tabs Help
rene.pihlak@lx18:~
vegan@vegan-HDD ~/Documents/TTU/LATEX/...
1.1) Cadence 2018 EDA version w/ AMS HITKIT 4.11 0.18um designkit
2) Mentor Graphics 2017 EDA version
2.1) Mentor Graphics 2018 EDA version
3) Synopsys 2017 EDA version
3.1) Synopsys 2018 EDA version
3a) Synopsys 2018 TETRAMAX standalone N-2017.09-SP5
4) XILINX Vivado Design Suite 2017.3
4.1) XILINX Vivado Design Suite 2018.1
5) ARM DS-5 Development Studio v5.28.1
0) Old legacy CAD versions selection..
q) no selection
----> 2.1

# Setting Up Lab Computer

Several paths, etc will be loaded. You are now ready to launch Questa Sim.


rene.pihlak@lx18:~
File Edit View Search Terminal Tabs Help
rene.pihlak@lx18:~
vegan@vegan-HDD ~/Documents/TTU/LATEX/...
Loading HDL-DESIGNER_2017.1 .. done.
Loading HL-3DEM_15.3_RH .. done.
Loading HL-DRC_6.5.U1_RH .. done.
Loading HL-SI-PI-TH_9.4.2_RH .. done.
Loading LEONARDO_2017a .. done.
Loading PRECISION_2017.1 .. done.
Loading PYXIS_10.5-7 .. done.
Loading QUESTA-CDC-FML_10.6c-1_RH .. done.
Loading QUESTA-CORE-PRIME_10.6c-1 .. done.
Loading QUESTA-INFACT_10.6c-1 .. done.
Loading REQTRACER_2017.1 .. done.
Loading TESSENT_2017.4 .. done.
Loading VISTA_2017.07_RH .. done.
Loading VISUAL-ELITE_4.7.0 .. done.
Loading VISUALIZER_10.6c-1 .. done.
Loading X-ENTP-VX_2.2_RH .. done.
All done.
Environment ready for Mentor Graphics 2018 EDA version.
/home/rene.pihlak> vsim

## Setting Up Linux Environment

# Setting up a project in Questa Sim

- Launching Questa Sim
- Create project and compile design files

# Using Command Line to Launch Questa Sim

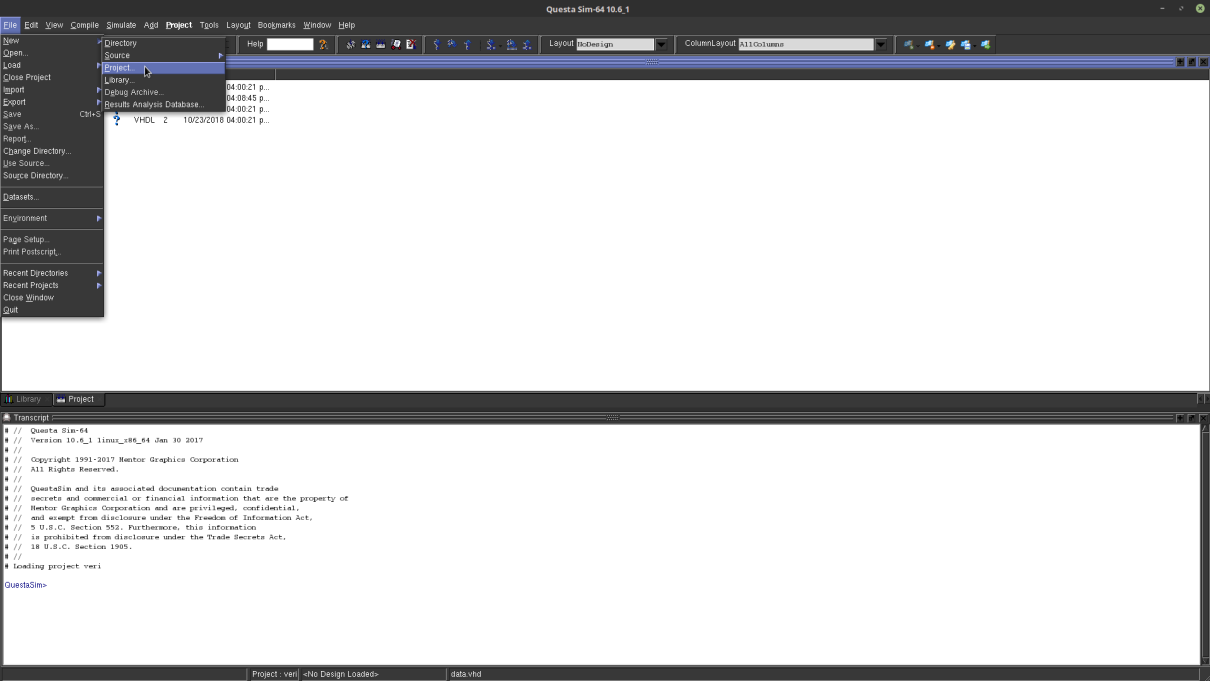
Questa Sim is launched by the following command:

```
vsim
```

It is advisable to launch Questa Sim in some project folder as it will generate several files and it is easier to keep track on all the necessary files if the working directory does not include other unrelated files and folders.
Also keep in mind that all files not saved to your P drive can (and will be) deleted after you log out.

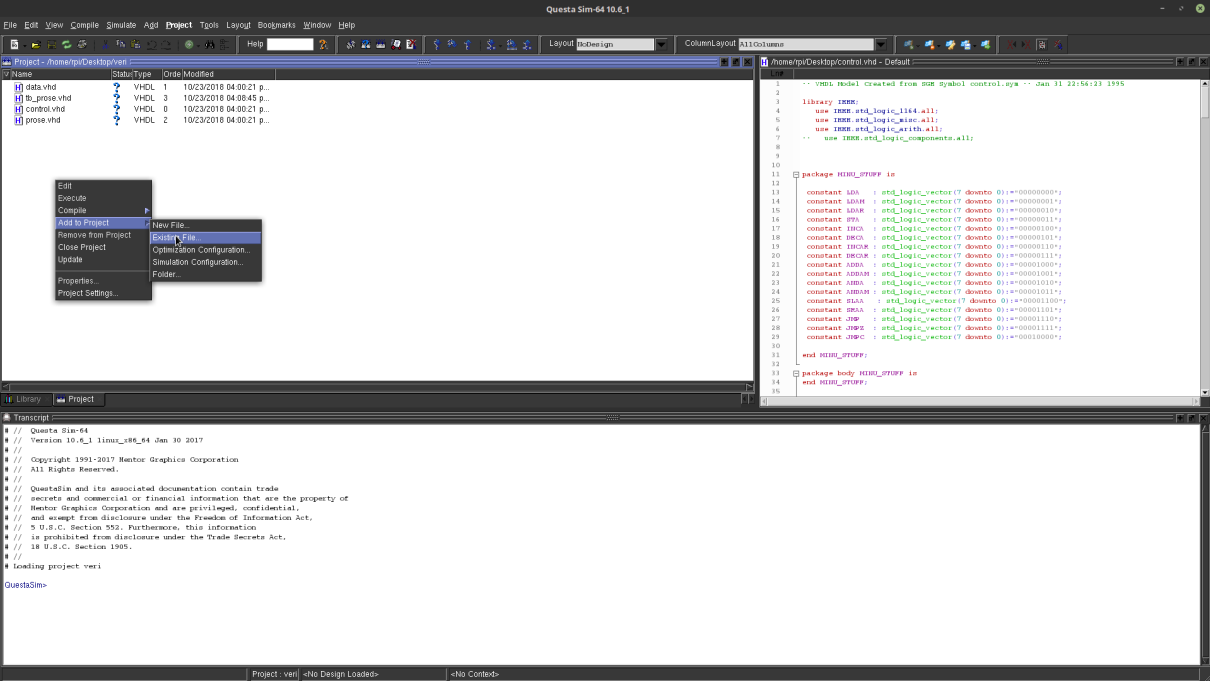
# Create a New Project

Create a new project.


Questa Sim-64 10.6_1
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
New
Open...
Load
Close Project
Import
Export
Save Ctrl+S
Save As...
Report...
Change Directory...
Use Source...
Source Directory...
Datasets...
Environment
Page Setup...
Print Postscript...
Recent Directories
Recent Projects
Close Window
Quit
Directory
Source
Project...
Library...
Debug Archive...
Results Analysis Database...
Help
Layout
DsDesign
ColumnLayout
AllColumns
VHDL 2 10/23/2018 04:00:21 p...
Library
Project
Transcript
# // Questa Sim-64
# // Version 10.6_1 linux_x86_64 Jan 30 2017
# //
# // Copyright 1991-2017 Mentor Graphics Corporation
# // All Rights Reserved.
# //
# // QuestaSim and its associated documentation contain trade
# // secrets and commercial or financial information that are the property of
# // Mentor Graphics Corporation and are privileged, confidential,
# // and exempt from disclosure under the Freedom of Information Act,
# // 5 U.S.C. Section 552. Furthermore, this information
# // is prohibited from disclosure under the Trade Secrets Act,
# // 18 U.S.C. Section 1905.
# //
# Loading project veri
QuestaSim>
Project : veri
<No Design Loaded>
data.vhd

# Add Files to the Design

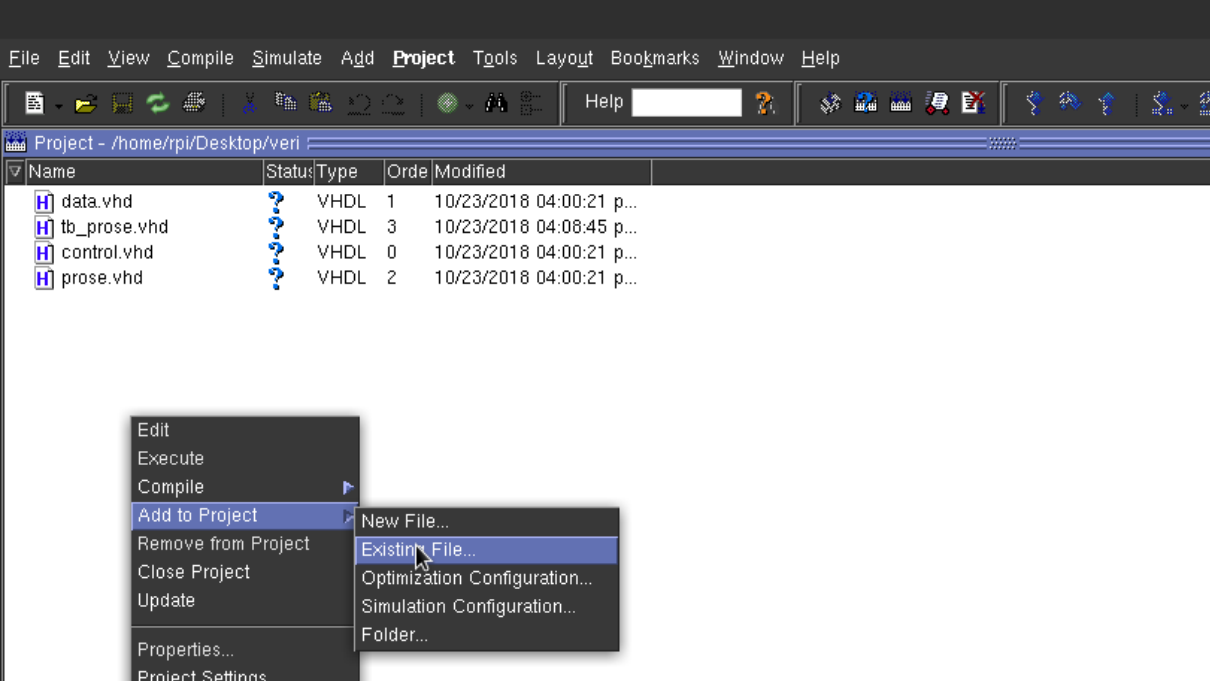
Right click on the project window and add your design files to the project. Select all the files in your design.


Questa Sim-64 10.6_1
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
Project - /home/rpi/Desktop/veri
Name Status Type Orde Modified
data.vhd ? VHDL 1 10/23/2018 04:00:21 p...
tb_prose.vhd ? VHDL 3 10/23/2018 04:08:45 p...
control.vhd ? VHDL 0 10/23/2018 04:00:21 p...
prose.vhd ? VHDL 2 10/23/2018 04:00:21 p...
Edit
Execute
Compile
Add to Project
Remove from Project
Close Project
Update
Properties...
Project Settings...
New File...
Existing File...
Optimization Configuration...
Simulation Configuration...
Folder...
Library
Project
/home/rpi/Desktop/control.vhd - Default
-- VHDL Model Created from RGM Symbol control.sym -- Jan 31 22:56:23 1995
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_misc.all;
use IEEE.std_logic_arith.all;
-- use IEEE.std_logic_components.all;
package MIHU_STUFF is
constant LDA : std_logic_vector(7 downto 0):="00000000";
constant LDAH : std_logic_vector(7 downto 0):="00000001";
constant LDAR : std_logic_vector(7 downto 0):="00000010";
constant STA : std_logic_vector(7 downto 0):="00000011";
constant INCA : std_logic_vector(7 downto 0):="00000100";
constant DECA : std_logic_vector(7 downto 0):="00000101";
constant INCAR : std_logic_vector(7 downto 0):="00000110";
constant DECAR : std_logic_vector(7 downto 0):="00000111";
constant ADDA : std_logic_vector(7 downto 0):="00001000";
constant ADDAR : std_logic_vector(7 downto 0):="00001001";
constant AMDA : std_logic_vector(7 downto 0):="00001010";
constant AMDAR : std_logic_vector(7 downto 0):="00001011";
constant SLAA : std_logic_vector(7 downto 0):="00001100";
constant SRAA : std_logic_vector(7 downto 0):="00001101";
constant JMP : std_logic_vector(7 downto 0):="00001110";
constant JMPZ : std_logic_vector(7 downto 0):="00001111";
constant JMPC : std_logic_vector(7 downto 0):="00010000";
end MIHU_STUFF;
package body MIHU_STUFF is
end MIHU_STUFF;
Transcript
# // Questa Sim-64
# // Version 10.6_1 linux_x86_64 Jan 30 2017
# //
# // Copyright 1991-2017 Mentor Graphics Corporation
# // All Rights Reserved.
# //
# // QuestaSim and its associated documentation contain trade
# // secrets and commercial or financial information that are the property of
# // Mentor Graphics Corporation and are privileged, confidential,
# // and exempt from disclosure under the Freedom of Information Act,
# // 5 U.S.C. Section 552. Furthermore, this information
# // is prohibited from disclosure under the Trade Secrets Act,
# // 18 U.S.C. Section 1905.
# //
# Loading project veri
QuestaSim>
Project : veri
<No Design Loaded>
<No Context>

# Example Project

The example design contain the following files:

- `data.vhd`
- `tb_prose.vhd`
- `control.vhd`
- `prose.vhd`


File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
Help
Project - /home/rpi/Desktop/veri
Name Status Type Orde Modified
data.vhd VHDL 1 10/23/2018 04:00:21 p...
tb_prose.vhd VHDL 3 10/23/2018 04:08:45 p...
control.vhd VHDL 0 10/23/2018 04:00:21 p...
prose.vhd VHDL 2 10/23/2018 04:00:21 p...
Edit
Execute
Compile
Add to Project
Remove from Project
Close Project
Update
Properties...
Project Settings
New File...
Existing File...
Optimization Configuration...
Simulation Configuration...
Folder...